Amendments to Specification

Please change the title to the following:

Data Transmission Across Asynchronous Time Domains Using Phase-Shifted Data Packet

Please amend the paragraph beginning on page 7, line 15 as follows:

Selection logic **300** is equipped to receive the above-referenced output signal (SEL) from delay circuit **302**, the input data signal (DATA), and the output data signal from delay circuit **304** (DATA'). Additionally, selection logic is equipped to receive an output clock signal that is asynchronous with respect to reference signal **306**. In accordance with the teachings of the present invention, selection logic **300** samples ~~bothDATA~~ both DATA and DATA' based on the output clock and selects one of the data lines such that during each transition of the output clock, valid data is present on the selected data line. In one embodiment, selection logic **300** selects between data lines (DATA, DATA') based at least in part upon the output of delay circuit **302** (SEL).